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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,790	09/26/2003	John Banning	TRAN-P243	9488

7590 12/20/2006  
WAGNER, MURABITO & HAO LLP  
Third Floor  
Two North Market Street  
San Jose, CA 95113

EXAMINER
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PAN, DANIEL H

ART UNIT	PAPER NUMBER
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2183

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	Application No. 10/672,790	Applicant(s) BANNING ET AL.	
	Examiner Daniel Pan	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 October 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-45 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

1. Clams 1-45 remain for examination.
2. Claims 1,17,18,23,33,37 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.
2. Claims 1-5,8,9-14,18, 17, 20,21-23, 34-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Nunomura (6,871,274).
3. As to the newly amended feature of fetching from memory, Nunomura also taught fetching from memory (see fig.5 [memory 250]).
4. As to the newly amended feature of executing on said processor, examiner holds that this does not change the original scope of the claim because execution has to be done by a processor.
5. Claims 6,7, 16,23-27, 32, 38,39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nunomura (6,871,274) in view of Rim (6,202,143).
6. Claims 28-31,40-44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nunomura (6,871,274) in view ) in view of Rim (6,202,143) in view of Ebicioglu et al. (6,112,299).
7. The rejections are maintained and incorporated by reference the last Office action on 06/26/06.
8. The response filed on 10/03/06 has been fully considered but is not persuasive.
9. In the remarks, applicant argued that :

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a) a bit pattern represents physical electrical or magential signals, and modifying of the recited bit patterns represents a physical transformation;

b) executing instructions on a processor is the foundation of application software and operating system software that supports it;

c) Nunomura teaches that such compressed instruction code is accessed by an instruction code conversion apparatus and not by an instruction decode unit, as are other machine language instructions;

d) compressed code is not a machine language instruction;

e) compressed code is unrecognizable as an instruction code (col.7, lines 30-37);

f) no modifying said instruction segment in Nunomura;

g) claim 1's instruction segment cannot be both four bits and 24 bits long;

h) claim 2 recites substitute a bit pattern od a subset of the instruction segment while Nunomura teaches substituting more bits than an instruction segment contains;

i) compressed code do not fairly suggest microcode;

j) no queue structure in Nunomura ;

k) no pointer in Nunomura;

l) a table mapping an index to a non-compressed code does not teach or suggest identifying a portion of an instruction for modification;

m) complexity of Rim in contrast to the relative simplicity of Nunomura would not have motivated to combine the references;

n) no desirability of Nunomura to accept VLIW;

o) consideration of the whole of the teachings of Nunomura and Rim, one of

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ordinary skill in the art would not be motivated to modify a decompression

process with a process that stuffs meaningless filler into an instruction word;

p) Nunomura has no need for the filler methods of Rim, as Nunomura has a single bus and a single bus width;

q) Nunomura's intention is to reduce the size of compressed instruction codes. Hence Nunomura teaches away from the recited fetching of VLIW machine language instructions as recited in claim 6;

r) By teaching hardware units hard-wired to specific bit positions, Ebicioglu teaches away from embodiments of the present invention that recite a "trigger pattern identifies an arithmetic logic unit segment" as recited by Claim 28.

10. As to a) above, electrical and magnetic signals are the natural phenomenon, therefore it is non-statutory (see MPEP 2105, 2100-10). As to the bit patterns, bit patterns are the states of the signals, therefore, non-statutory.

11. As to b) no application software nor operating system can be found in the claim. Applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)).

12. As to c), d), Nunomura taught that compressed instruction code was accessed by an instruction code conversion apparatus (see col.2, lines 1-2) and not by an instruction decode unit (see col.5; lines 6-20), as are other machine language instructions, and therefore, the compressed code was a machine language instruction.

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13. As to e), applicant never recites unrecognizable, or the like, see citation in "As to b) above".

As to f), Nunomura taught modifying said instruction segment (see Page 4, item b of the last office action on 06/26/06).

14. As to g), claim 1 never recites that the instruction segment cannot be both four bits and 24 bits long. See As to b) above.

15. As to h), claim 2 recites substitute a bit pattern of a subset of the instruction segment and Nunomura teaches substituting more bits than an instruction segment contains (see the corresponding index in fig.2 [index]). Therefore, Nunomura substituted a bit pattern [index] of a subset of the instruction segment.

16. As to I), Nunomura taught microcode (e.g. see fig.4 ['1' and 0']).

17. As to j), Nunomura taught a queue structure (see the entries of conversion table storing the instruction modification information in fig.2 [table entries]). No specific type of queue is being reflected into the claim. Therefore, it is read as any queue contains entries in general.

18. As to k), Nunomura taught pointer (see the index for corresponding instruction modification information in fig.2, see also co1.9, lines 39-40 for alternative embodiment).

19. As to l), Nunomura taught a table mapping an index to a non-compressed code therefore, it identified a portion of an instruction for modification (see the mapping in fig.2 [index]).

20. As to m), applicant failed to explain why the complexity of Rim in contrast to the relative simplicity of Nunomura would not have combined the references. However,

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examiner would like to point out the complexity of Rim in addition to the relative simplicity of Nunomura would have motivated one of ordinary skill in the art to combine the references, and the reasons of obviousness were already given in Page 6, paragraph 24 of the last Office action on 06/26/06, therefore, it will not be repeated herein.

21. As to n), no specific type of VLIW has been reflected into the claim. Therefore, one of ordinary skill in the art should be able to recognize the use of VLIW in general. The question to be asked is what is so special about applicant's VLIW ? Is applicant trying to say that one of ordinary skill in the art don't know VLIW ? Applicant's claim is silent about this question.

22. As to o), applicant failed to explain what does "stuffs meaningless filler " mean ?

23. As to p), applicant failed to explain why Nunomura's single bus and a single bus width has no need for the filler methods of Rim ?

24. As to q), Nunomura's intention is to minimize the length of compressed instruction codes. Therefore, Nunomura suggested the need for reducing the very large instruction code, such as size of VLIW.

25. As to r), Ebicioglu taught that each parcel 510 occupies specific bit positions and controls those hardware units hard-wired to those positions (col.11 lines 15-36). The hardware units hard-wired to specific bit positions was a trigger pattern which identified the arithmetic logic unit segment as claimed.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should



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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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